## CLAIMS

What is claimed is:

1. A recessed-bond semiconductor package substrate comprising:

a first metal layer;

an underlying metal layer; and

a dielectric layer between the first metal layer and the underlying metal layer, wherein the underlying metal layer is configured for a direct interconnection, through the first metal layer and the dielectric layer, with a semiconductor die.

2. The semiconductor package substrate of claim 1, wherein the direct interconnection is formed by at least one bond wire.

3. The semiconductor package substrate of claim 1, wherein at least one opening is created through the first metal layer, exposing a portion of the die for receiving the bond wires.

4. The semiconductor package substrate of claim 3, wherein the underlying metal layer comprises a signal layer.

5. The semiconductor package substrate of claim 4, wherein the first metal layer comprises a ground plane.

6. The semiconductor package substrate of claim 4, wherein the signal layer is sandwiched between a pair of the dielectric layers.

7. The semiconductor package substrate of claim 1, wherein the plurality of metal layers comprise copper.

8. The semiconductor package substrate of claim 1, wherein the plurality of dielectric layers comprise bismaleimide triazine (BT)

9 A method for assembling a semiconductor die onto a package substrate, the method comprising:

attaching the die over a top metal layer of the substrate; and

wirebonding the die to an underlying metal layer of the substrate.

10. The method of claim 9, wherein the substrate is configured with at least one opening, exposing a portion of the underlying metal layer for receiving at least one bond wire.

11. The method of claim 10, wherein the underlying metal layer comprises a signal layer.

12. The method of claim 11, further comprising molding an encapsulant over the die.

13. The method of claim 11, further comprising attaching a plurality of solder balls to the substrate.

14. The method of claim 11, wherein the top metal layer comprises a ground plane.

15. The method of claim 11, wherein the signal layer is disposed between a pair of dielectric layers.

16. A packaged semiconductor device comprising:

an integrated circuit die; and

a package substrate, wherein the package substrate further comprises:

a plurality of metal layers, wherein the metal layers are separated by a dielectric layer, the metal layers further comprising:

an *n* metal layer;

an *n-1* metal layer, wherein the *n-1* metal layer is connected to the die by a plurality of bond wires;

an *n-2* layer; and

an *n-3* layer.

17. The device of claim 16, wherein the *n-1* layer comprises a plurality of signal traces.

18. The device of claim 17, wherein a ground plane is disposed above the signal traces.

19. The device of claim 18, wherein the signal traces are sandwiched between a pair of the dielectric layers.

20. The device of claim 19, wherein one of the pair of the dielectric layers is a substrate core layer.

21. The device of claim 18, wherein the *n-2* metal layer comprises a power plane.

22. The device of claim 18, wherein the *n-3* metal layer comprises a land layer.